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REMARKS

This amendment is being filed in response to the Office Action dated September 14, 2005. For the following reasons, this application should be considered in condition for allowance and the case passed to issue.

Claim 6, 7 and 10 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. In particular, the trademark name "SilK" was employed in Claim 6. This has been corrected by the amendment made to claim 6 to employ the term "poly-arylene ether." This change does not add new matter to the application since SilK is known to be a poly-arylene ether. (See, for example, the cited Uzoh reference at Col. 3, line 39). Accordingly, reconsideration and withdrawal of the rejection of claims 6, 7, and 10 under 35 U.S.C. §112, second paragraph are respectfully requested.

Claims 1-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Uzoh et al. (hereafter "Uzoh") and further in view of Gaw et al. (hereafter "Gaw"). This rejection is hereby traversed and reconsideration and withdrawal thereof are respectfully requested.

The following is a comparison of the present invention as currently claimed with the Uzoh and Gaw combination.

As provided, for example, in amended claim 1, the invention provides for a method of forming an interlevel dielectric (ILD) layer. This method comprises the steps of forming a polymer sacrificial ILD on a substrate and a photomask on the polymer sacrificial ILD. Recesses are etched in the polymer sacrificial ILD through the photomask. Metallization structures are formed within the polymer sacrificial ILD while the photomask is on the polymer sacrificial ILD. This includes depositing copper within the recesses in the polymer sacrificial ILD and forming a metal cap layer on the copper deposited within the recesses. The polymer sacrificial ILD is etched back. Dielectric

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material is non-conformally deposited as an ILD layer over the substrate and the metallization structures supposed to form air gaps in the ILD layer between at least some of the metallization structures.

As provided in independent claim 11, for example, the invention provides for a method of forming an interconnect structure comprising the steps of forming a polymer into an interlevel dielectric (ILD) layer on a substrate. A photomask is formed on the polymer ILD layer and recesses are etched in the polymer ILD layer through the photomask. Metal lines are formed within the polymer ILD layer. These metal lines are capped with a cap layer while the photomask is on the polymer ILD layer. The photomask is removed and the polymer ILD layer is etched back. Subsequently, a second ILD layer is formed on the substrate.

By maintaining the photomask on the polymer's sacrificial ILD during the formation of the metallization structures (including metal caps), the likelihood of copper sputtering from the top of the metal lines is greatly reduced. The maskless process for etching back the sacrificial ILD can be employed since the polymer sacrificial ILD has a chemical bonding that is much weaker than silicon-oxide bonding and the silicon dioxide of conventional processes. This results in simplified manufacturing and reduced costs, as well as improving the accuracy and efficiency of the process. Neither Uzoh nor Gaw show or suggest such method steps, such that the combination of Uzoh and Gaw does not show or suggest the invention as now claimed.

Uzoh, U.S. Patent No. 6, 413, 854, relates to a method of building a multi-level structure and describes a process, such as that shown in Figures 5-9. In this process, as seen especially in Figures 7-9, the recesses are formed in the dielectric layer 13 and a photomask is removed. The metal 19 is only then deposited over the dielectric layer 13 and barrier/adhesion layer 17, and polished to achieve the structure of Figure 9. Figure 12 shows a structure in which the dielectric

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layer has been removed and caps are employed over the copper. However, the formation of the metal caps is not detailed and there is no suggestion for forming the caps while the photomask is in place on the polymer ILD layer. Hence, Uzoh is subject to the same concerns of misalignment as depicted in the prior art of Figures 1-3 described in the present application.

Gaw, U.S. Patent No. 6,303,464, relates to a method and structure for reducing interconnect system capacitance through encased voids in a dielectric layer. While discussing air gaps or voids in an ILD, Gaw fails to overcome any of the deficiencies noted above with respect to the Uzoh reference. In particular, Gaw fails to describe the formation of caps on metal lines while a photomask is in place on the polymer ILD layer. Likewise, Gaw does not provide any suggestion as to how to overcome the misalignment concerns of a cap or photoresist masks on the copper or metal lines.

Since neither Uzoh or Gaw show or suggest the method steps of the invention as now claimed, such as forming of recesses into a polymer ILD layer through a photomask and forming metal lines with a cap layer while the photomask remains on the polymer ILD, the combination of these references cannot show or suggest the invention as now claimed in independent claims 1 and 11. Accordingly, reconsideration and withdrawal of the rejection of claims 1 and 11, and those claims dependent therefrom, are respectfully requested.

In light of the amendments and remarks above, this application should be considered in condition for allowance and the case passed to issue. If there are any questions regarding this amendment or the application, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including

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extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

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